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DP83848T-MAU-EK Purpose and Contents

The purpose of the DP83848T-MAU-EK (EK) is to provide National Semiconductor Corp.'s customers with a vehicle to quickly design and market systems containing the DP83848T chip. Customers are encouraged to copy EK components to expedite their design process.
The EK contains:

- DP83848T Media Attachment Unit (MAU)
- Printed copy of this User's Guide
- DP83848T MAU schematic
- DP83848T MAU licensing agreement

Information and Specifications

This section contains specifications of the DP83848T MAU card, as well as a description of the card's interfaces, connectors, jumpers and the LED.

Usage setup and configuration

Power for the DP83848T MAU is supplied via MII connector.

- If 5V is supplied, the on-board voltage regulator, U5, will convert 5V to 3.3V for the device. J11 should be removed.
- If 3.3V is supplied from the MII connector, J11 needs to be ON (See schematics for details).

Address settings:

The PMD address for the DP83848T Physical Layer device is set by jumper J4.

- Default board setting for the PHY Address is 01
- The board may be set to PHY Address 03 by adding jumper J4.

Table of jumpers:

Jumper	Name	Function
J1	MII Male Connector	MII interface
J2	MII Header	Alternative connection for MII signals
J3A,B,C	MDIO access	J3 A to B should be ON for MII MDIO access, J3B to C should ON for on_board uMDIO access, J3 A, B, C should be OFF for external uMDIO/FDI card use
J4	PHYAD1	PHY Address strap pin (PHY address = 01 when J4 is OFF, PHY address = 03 when J4 is ON)
J5	MDIX_EN	Auto_MDIX is enabled when J5 is OFF and disabled when J5 is ON.
J6	LED_CFG	Set LED configuration. When J6 is OFF and the chip is powered, a light on LED_LNK represents the presence of a link. When J6 is ON, the blinking light on LED_LNK represents link and activity. In both cases when there is no light on LED_LNK, this is an indication of absence of link.
J7	RESET_N	J7 ON will reset the device
J8 (Not populated)		
J9	Optional header	
J11	MII 3V3 option	J11 should OFF for 5V MII supply and J11 should be ON for 3.3V MII supply
J12	Pulse Jack	Integrated Magnetic RJ-45 connector
J15	MDIO connector	On_board uMDIO connection

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DP83848T MAU Specification

Overview

The DP83848T MAU is an NSC demo platform to allow customer evaluation of our device.
While the DP83848T has many advanced and enticing features, this specific board is designed to demonstrate *only* a subset of those. The features chosen are the ones that the mainstream customers will use. Thus we have created an affordable, aesthetic platform to demonstrate the simplicity of designing in a National Semiconductor DP83848T.

Target Environment

Any customer equipment that provides a standard IEEE 802.3, Clause 22 MII DTE interface; e.g. SmartBits/Netcom box.

Features/Goals

The DP83848T MAU features:

- Intergrated magnetics
- Minimum configuration requirements:
    - 2 PHY Addresses - 01h (default) or 03h
    - 2 LEDs – 1 power, 1 LED for LINK
    - Strap Options – MDIX_EN, LED_CFG
    - RESET_N jumper
- Connections for the following interfaces:
    - MII Interface
    - Integrated transformer RJ-45
    - Header for “ribbon cable” connection to MII
- Standard PCB layout considerations with regards to clock, MII, and TD/RD
- Single sided component placement
- On-board clock – Crystal
- On-board power supplied by MII connector *only*, jumper to configure 5v or 3.3v
- On-board MDIO circuit
- Low cost

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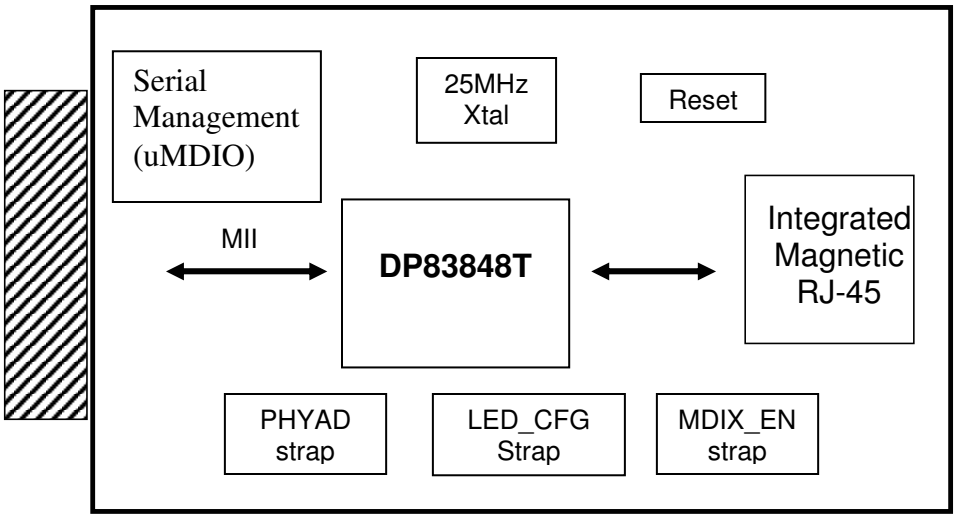
MAU Block Diagram



PCB Physical Layout requirements / Considerations

- FR4 material
- Trace impedance will be ensured by design:
  - Trace symmetry within differential pair (+/- 0.5")
  - Differential impedance 100 ohms, +/- 5%
  - Adjacent differential pairs spacing > 2X distance within a differential pair, to minimize cross-talk and EMI
- Trace length matching between differential pairs not required
- Trace space will be 0.007"/0.008" minimum
- Uniform supply & ground plane
- Combination of through-hole and surface mount technology
- Target size 2.0" (height), 3.0" (length)
- 4 layers
- Silk screen on two sides

MAU Interface requirements

- System interface will be via the MII connector, and MII header
- RJ-45 for network connection
- On Board Serial Management circuit

Software

- No device specific software is required for this board
  National does provide the integrity utility; a diagnostic and configuration package at
  www.national.com/appinfo/networks/ethernet_utility.html

Additional information

Updated versions of the included material, related material can be found by going to ethernet.national.com or directly to design resources at http://www.national.com/appinfo/networks/webench/dp83848.html

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